REMARKS

The Applicants appreciate the Examiner's thorough review of the present application, and respectfully request reconsideration in light of the forgoing amendments and the following remarks.

Claims 1-4 stand rejected under 35 U.S.C. §112 as failing to comply with the second paragraphs. After the above amendment, the amended claim 1 clearly point out that the channel length of each of the second MOS transistors is "larger" than that of each of the first MOS transistors. Accordingly, the Examiner is requested to withdraw the Section 112 rejection of claims 1-4.

Claims 1 and 3-4, insofar as in compliance with 35 U.S.C. §112, stand rejected under 35 U.S.C. §103(a) as being unpatentable over Takahashi et al. (US Patent No. 6,445,215) or Wollesen et al. (US Patent No. 5,828,110) in view of Ker et al. (US Patent No. 5,852,315). This rejection is respectfully traversed.

As per claim 1, the Examiner asserts that Takahashi et al. teach everything in claim 1 except that first and second MOS transistor arrays are surrounded by first and second guard rings, respectively. The Examiner also asserts that Wollesen et al. teach everything in claim 1 except a plurality of MOS transistors. Ker et al. teach first and second MOS transistor arrays comprising a plurality of MOS transistors and surrounded by first and second guard rings, respectively. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine their teachings.

However, what Takahashi et al. actually disclose in Fig. 1 is a multiple input logic circuit, which has nothing to do with ESD protection. In addition, the teaching of wider gate of the n-channel MOS transistor is to increase the current capacity to prevent the speed-down of the pull-up as much as possible, which is different from the claimed invention. In the claims, because of the longer channel, the potential enables second parasitic BJT to reach first breakdown and enter the snapback breakdown region is larger than that of first parasitic BJT.

Moreover, what Wollesen et al. teach is a latchup-proof I/O circuit, which also has nothing to do with ESD protection. Furthermore, the Examiner mentions Fig. 11 as evidence that the channel of first MOS transistor is longer than that of second MOS transistor. Fig. 11 is such an inaccurate figure and was provided just for the illustration of the inventive layout roughly. The variation of the channel lengths between two MOS transistors raised by the Examiner was not even mentioned in the specification, let alone taught or suggested.

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references or in the knowledge generally available to one having ordinary skill in the art, to combine the references. As the above argument, the Examiner fails to establish such a *prima facie* case of obviousness. Thus, claim 1 is considered patentable.

As per claim 3, the Examiner asserts that Takahashi et al. and Wollesen et al. teach gates of the first MOS transistors are electrically connected to each other, and so are those of the second MOS transistors, wherein the gates of the first MOS transistors are grounded, and so are those of the second MOS transistors.

However, in Fig. 1, Takahashi et al. teach signal B connecting with the gate of a n-MOS transistor(M22) and the gate of a p-MOS transistor(M24), and signal A connecting with the gate of a n-MOS transistor(M21) and the gate of a p-MOS transistor(M23). Thus Takahashi's teaching is different from this application. Moreover, Wollesen et al. teach only a p-MOS and a n-MOS. It is impossible for Wollesen et al. to teach the gates of the first and second MOS transistors respectively electrically connected. Thus claims 3 and 4 are considered patentable for at least the reasons set forth above.

As independent claim 1 is submitted to be patentable for the reasons set forth above, claim 2 depending from claim 1 is also submitted to be patentable.

A Notice of Allowance is therefore respectfully requested.

If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6903. If any other fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No JLINP093.DIV3). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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